

The diagram shows a system 1 consisting of multiple image processors (2) and a controller (3). Each image processor (2) includes an IMAGE PROCESSOR block and a small output block (4). The output blocks (4) of all image processors are connected to a common bus (A). This bus (A) is connected to a controller (3) via a line (5). The controller (3) is connected back to the image processors via a line (6).

FIG. 2

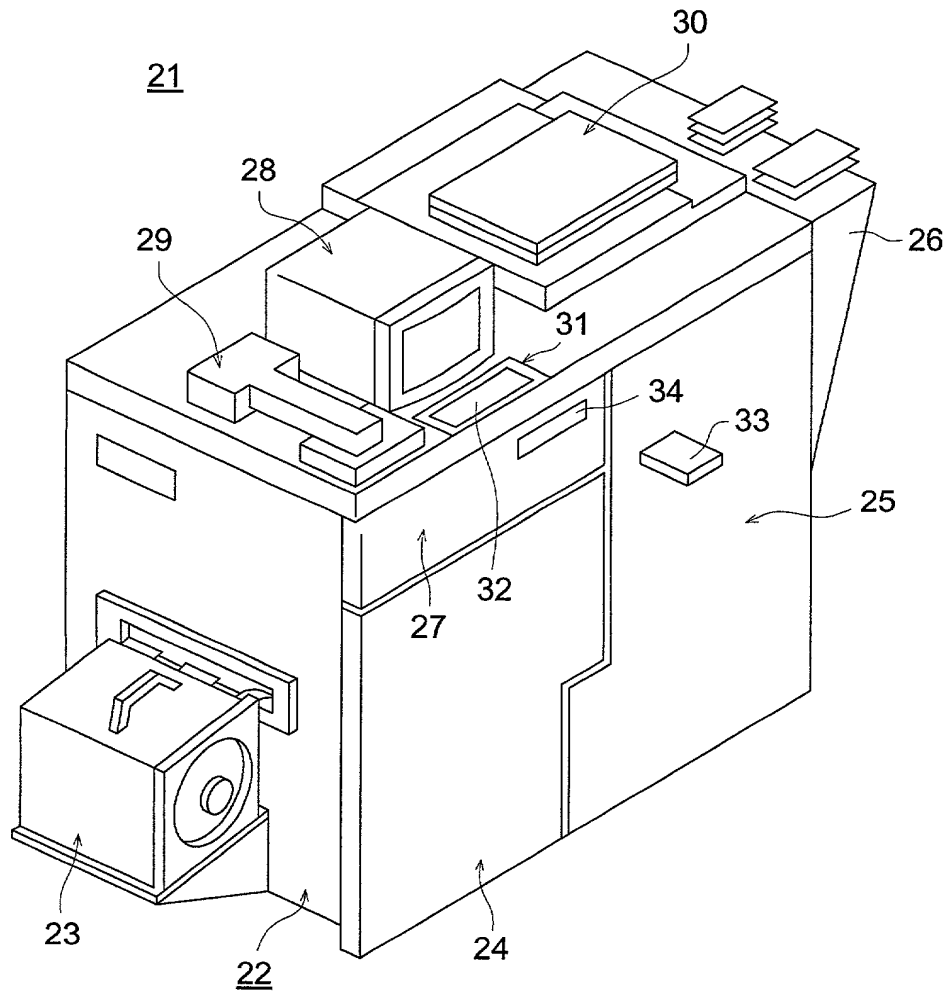


FIG. 3

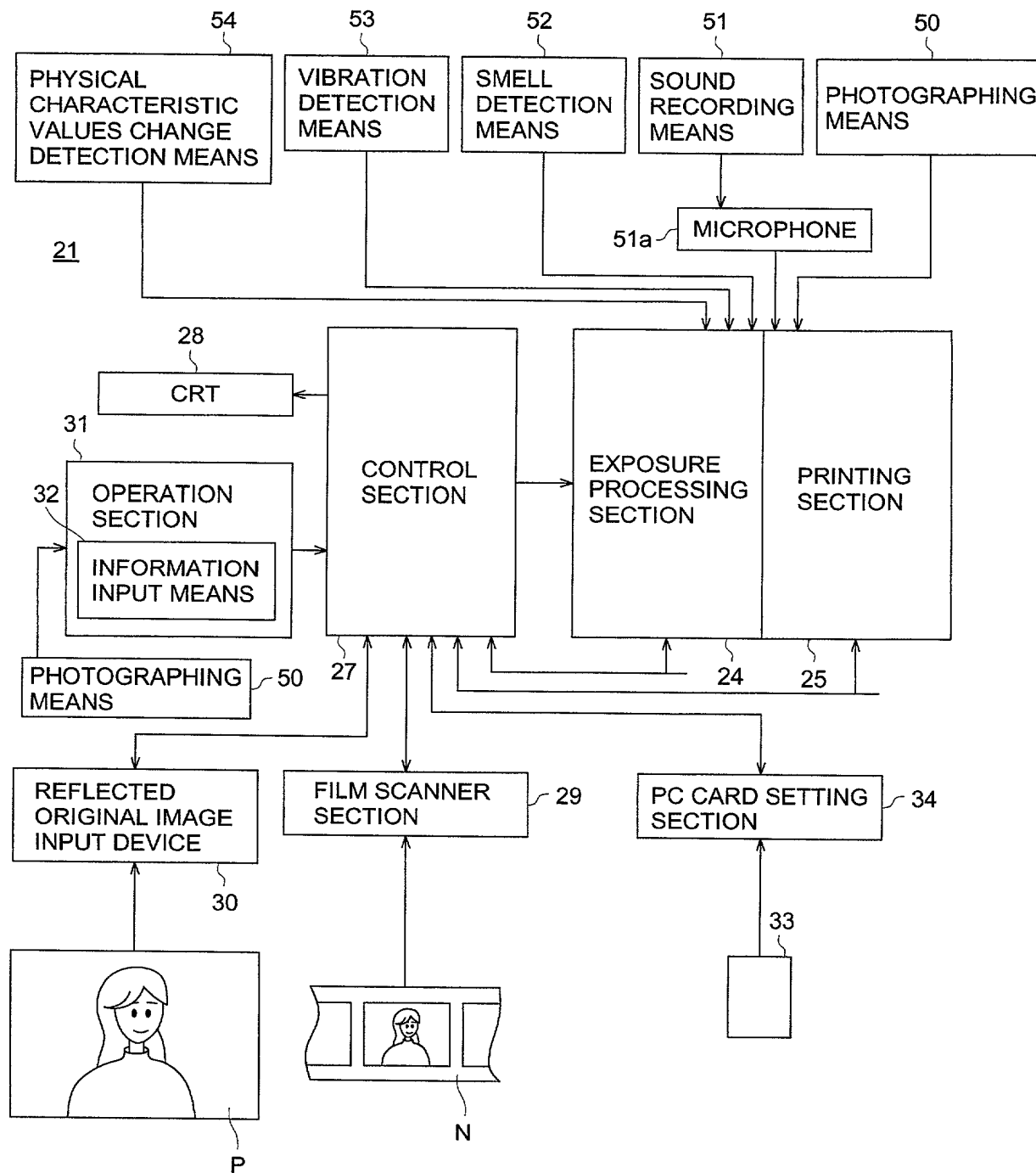


FIG. 4

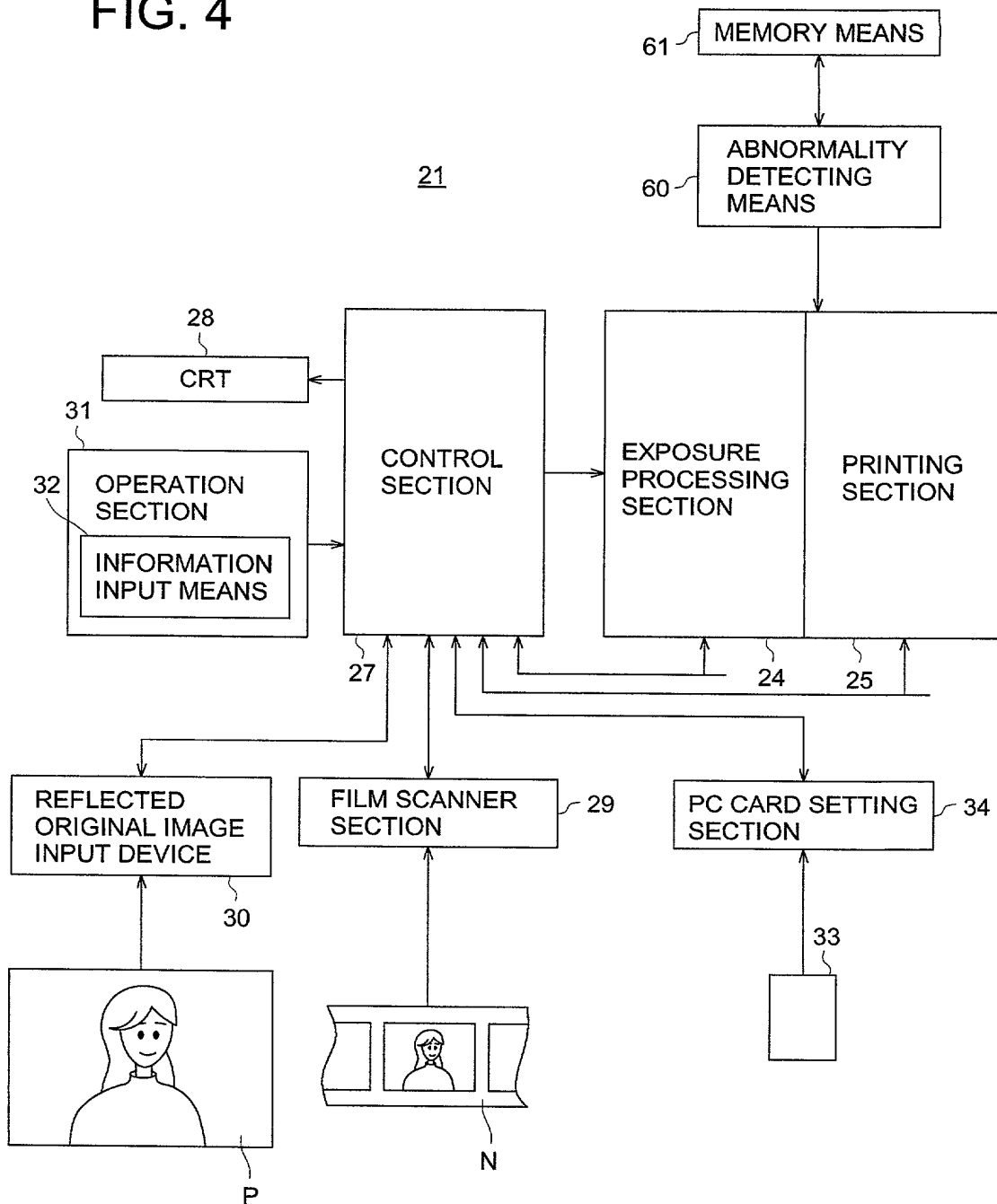


FIG. 5

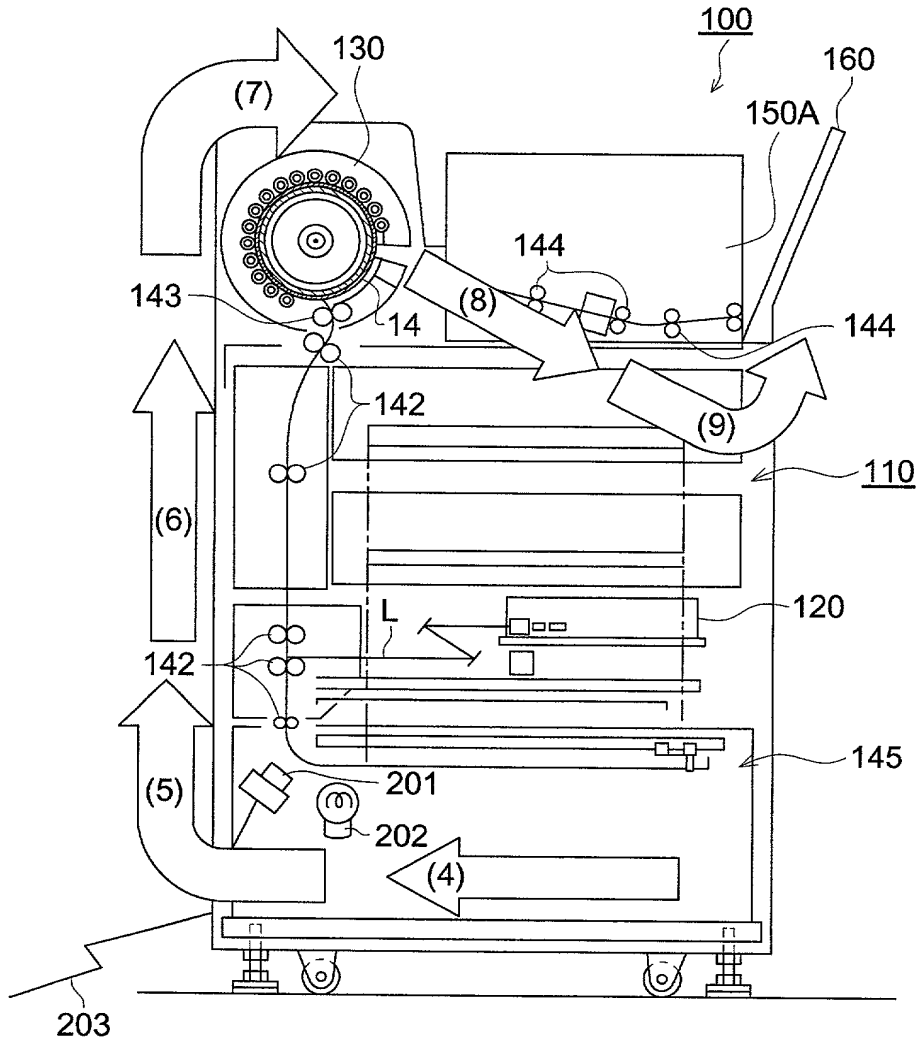


FIG. 6

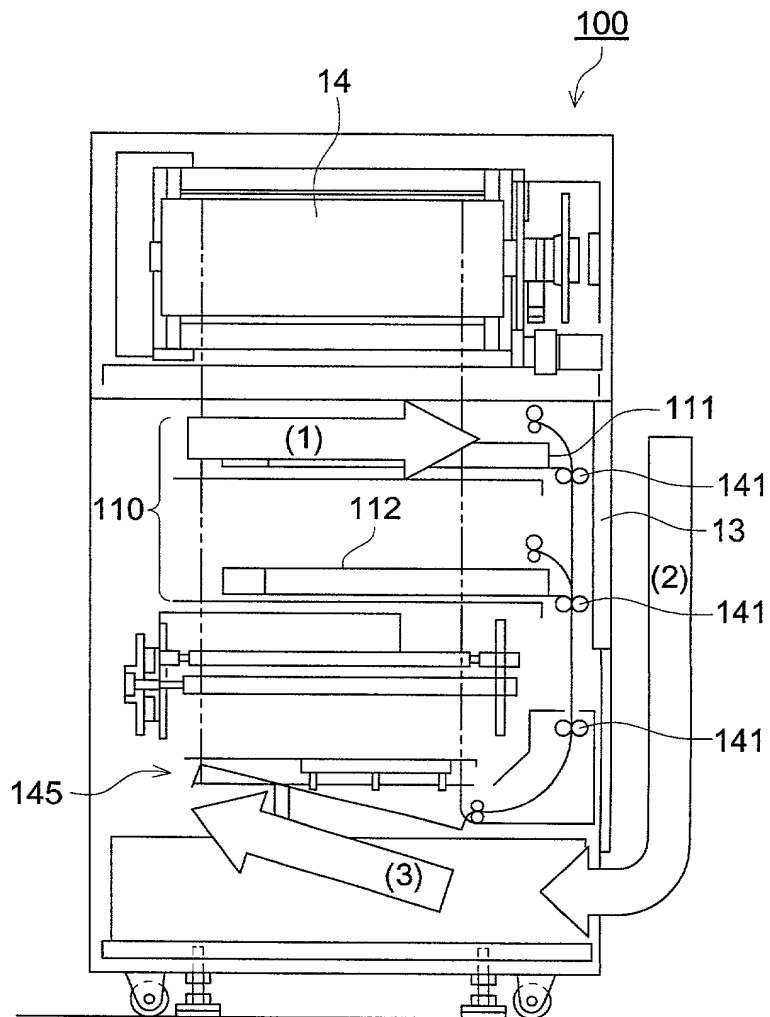


FIG. 7

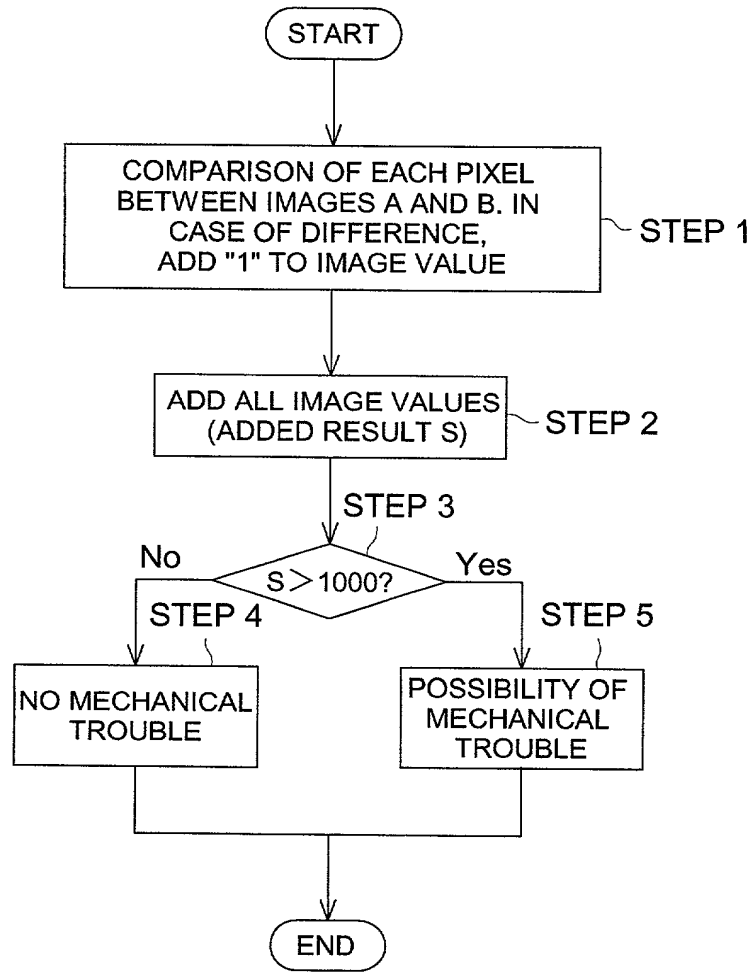


FIG. 8

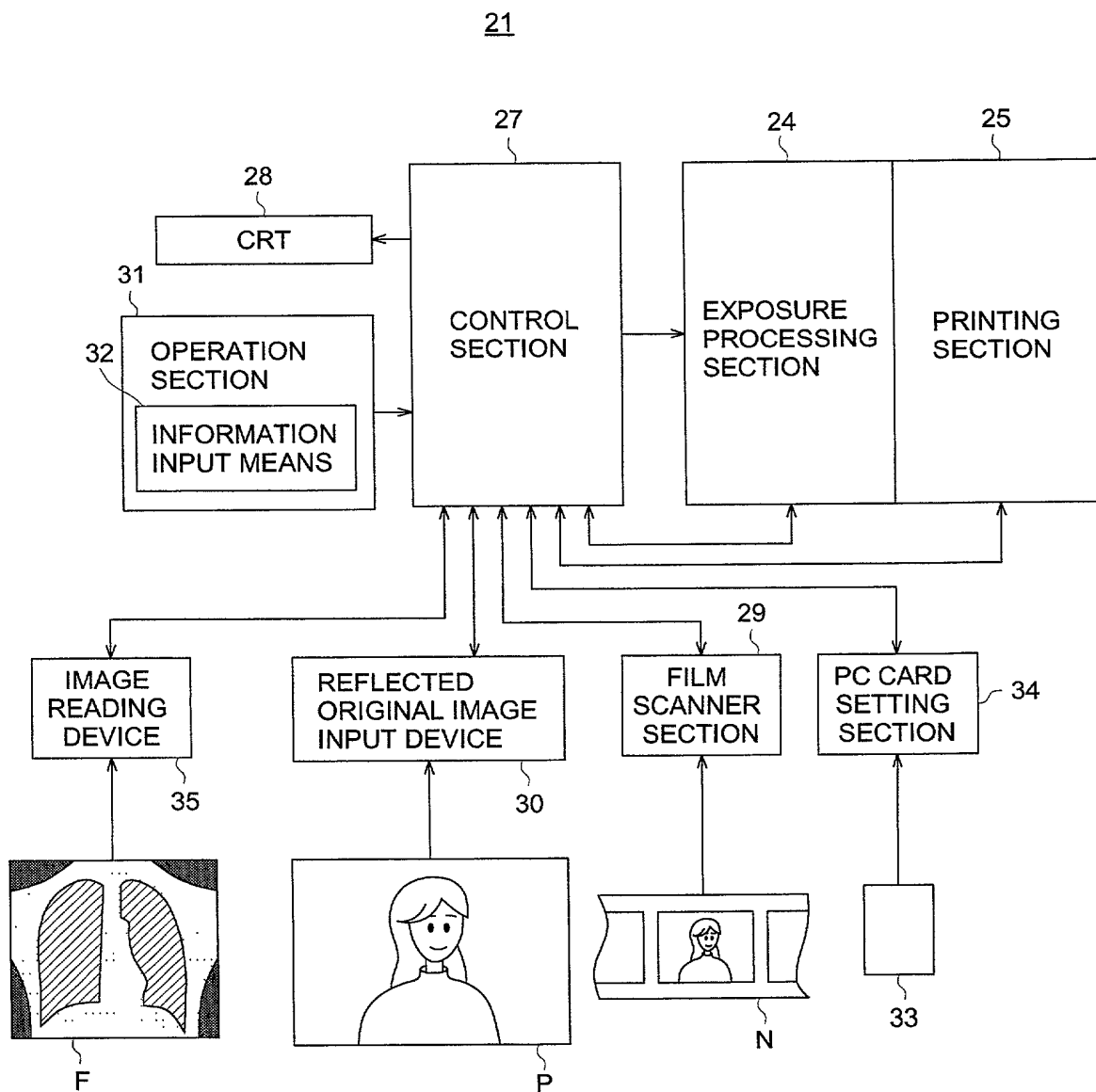




FIG. 9

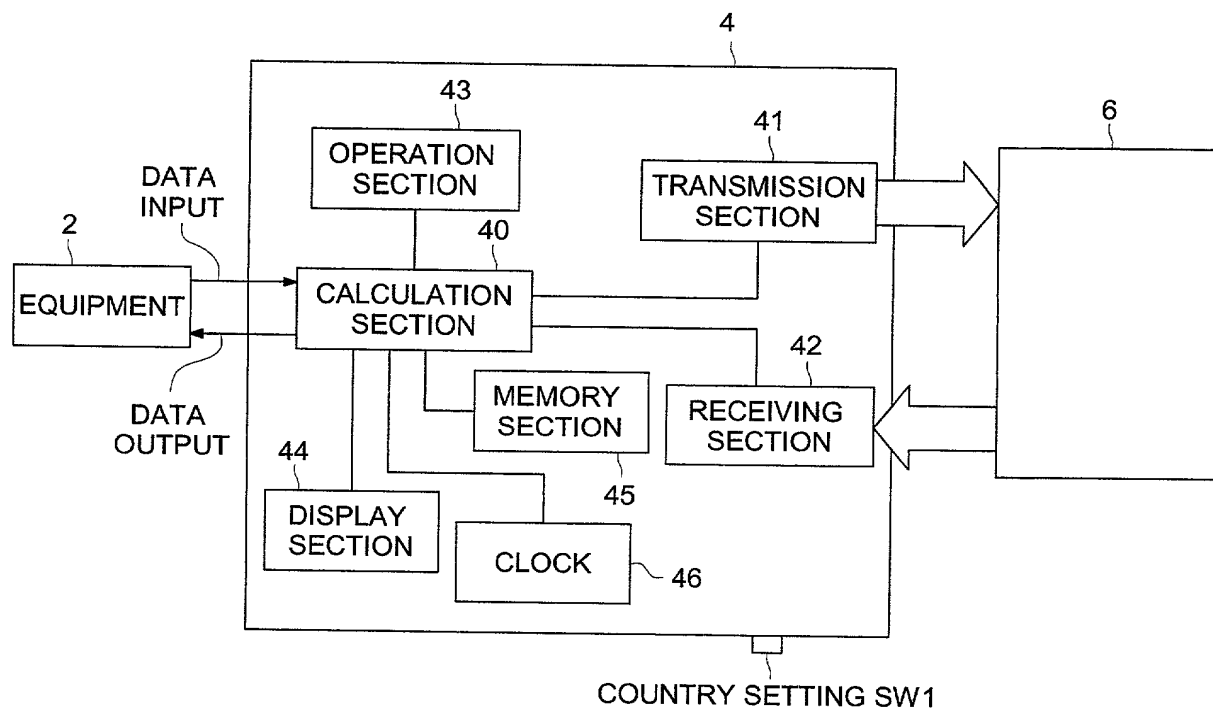


FIG. 10

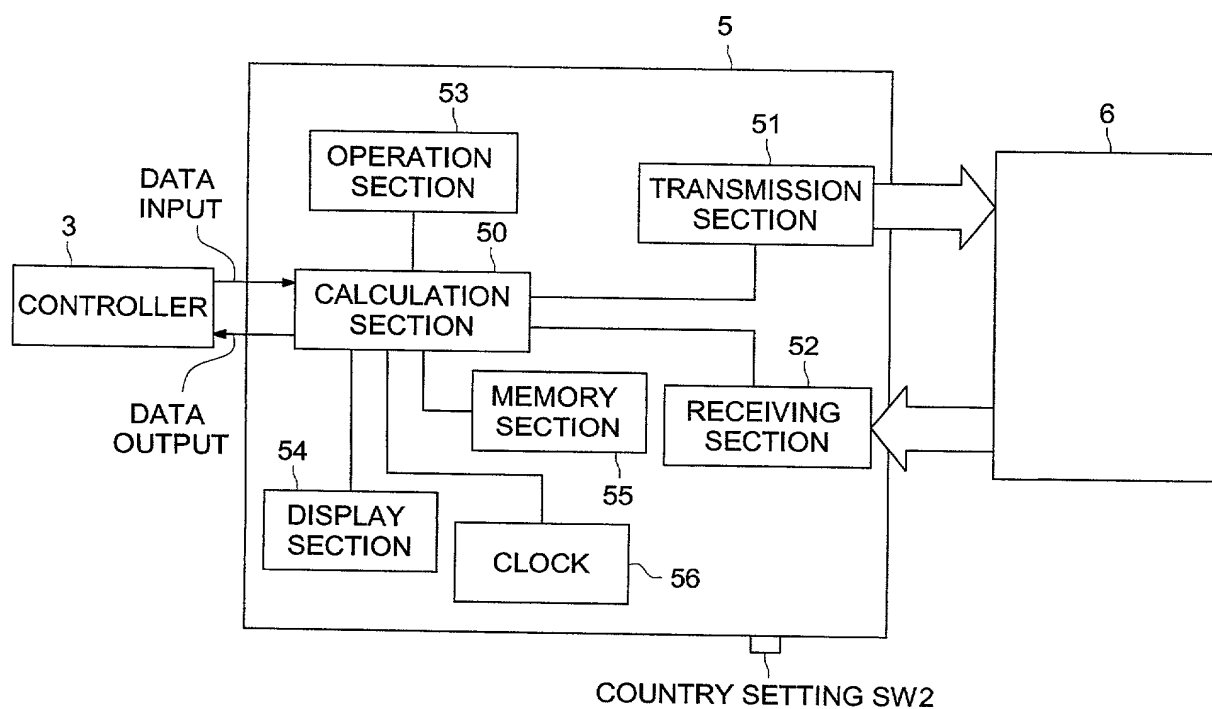


FIG. 11

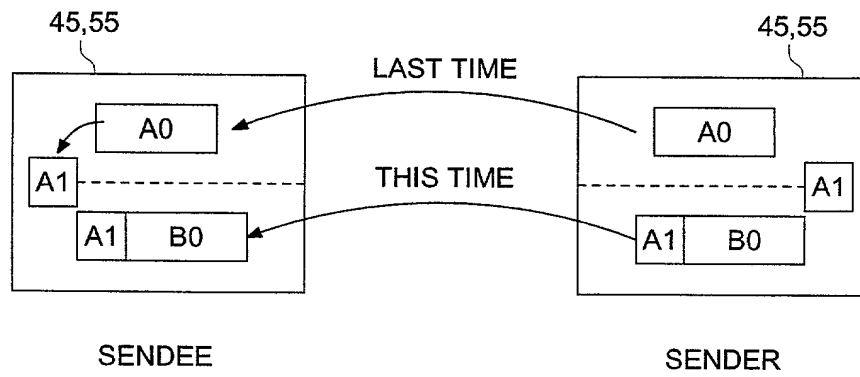


FIG. 12 (a)

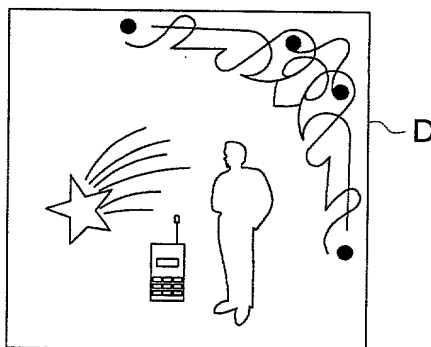


FIG. 12 (b)

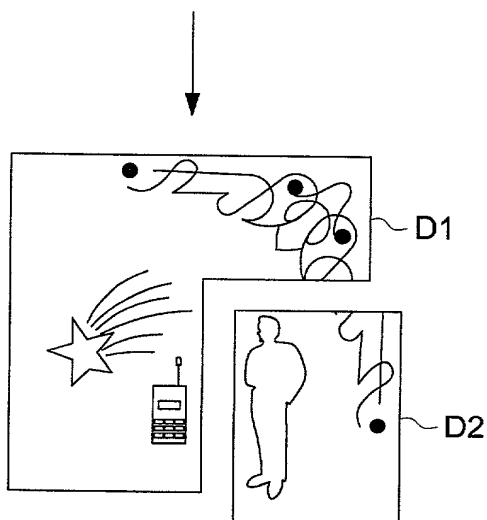


FIG. 12 (c)

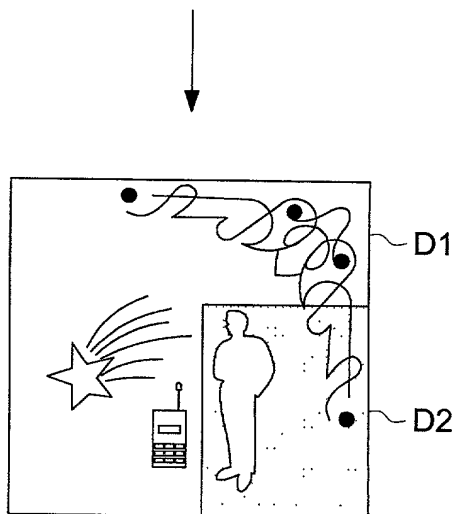


FIG. 13

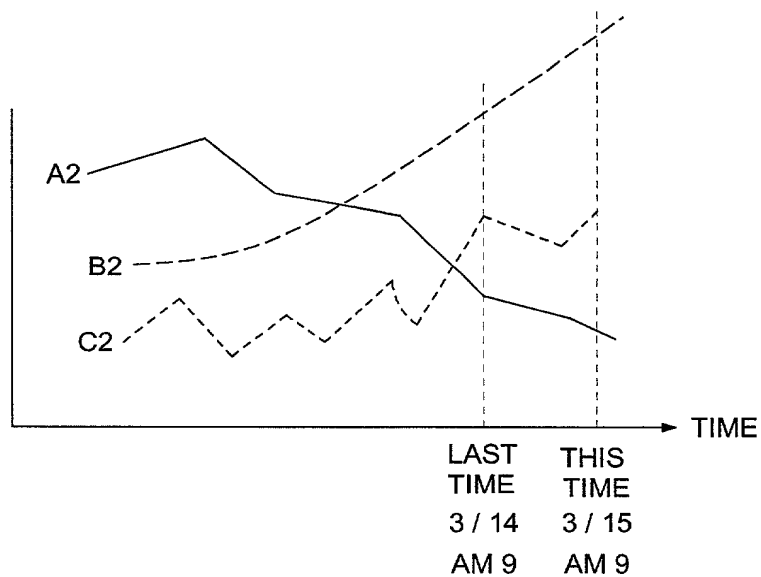


FIG. 14

